Applied Physics Seminar Series

Semiconductor nanowires for electronics and sensors

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Abstract: Metal-catalyzed semiconductor nanowires have been widely discussed and examined as self-assembled nanostructures, potentially compatible with the dominant silicon integrated-circuit electronics. Nanowires of the Group IV materials Si and Ge have been extensively studied, as have nanowires of many III-V and II-VI semiconductors. The growth processes have been widely investigated, and continued work is needed to find suitable catalyst materials compatible with Si electronics. Nanowires can grow horizontally from a vertical (111) plane etched from a (110)-oriented Si layer to form cantilever or bridging structures. These Si IC-compatible structures can be used as field-effect sensors or as resonant sensors for measuring chemical or biological species. Nanowires with typical dimensions resonate at convenient frequencies in the MHz range and with quality factors above 20,000 at low pressures. The epitaxial connection of the nanowires to the support post reduces mechanical losses at this connection. The resonant structures can be actuated electrically or piezoelectrically, and the response can be detected optically or electrically. Data suggest that the quality factor does not degrade greatly as the pressure increases to atmospheric pressure. Nanowires of compound semiconductors can be grown on Si and may be especially useful for optoelectronic applications. Because of the small contact area, the lattice mismatch does not seriously degrade the crystal quality of the growing nanowires. Electrical connection between the nanowires and the Si substrate needs attention. Metal-catalyzed nanowires have been suggested as the channels of advanced MOS devices and are included in the 2007 ITRS as a potential "emerging material". Many challenges remain, especially integrating a dense array of nanowires for high-performance, random logic.

Ted Kamins is Principal Scientist in the Information and Quantum Systems Laboratory at Hewlett-Packard Laboratories in Palo Alto, California, where he is conducting research on advanced nanostructured electronic and sensing materials and devices. He is also a Consulting Professor in the Electrical Engineering Department at Stanford Univ. He received his degrees from the Univ. of Cal., Berkeley. He then joined the Research and Development Laboratory of Fairchild Semiconductor, before moving to Hewlett-Packard, where he has worked on numerous semiconductor material and device topics. Ted is co-author with R. S. Muller of the textbook "Device Electronics for Integrated Circuits" and is author of the book "Polycrystalline Silicon for Integrated Circuits and Displays." He is a Fellow of the IEEE and of the Electrochemical Society. He taught at the Univ. of Cal., Berkeley, and at Stanford Univ. and has been an Associate Editor of the IEEE Transactions on Electron Devices.

Anyone interested in meeting with the speaker should contact ***Avi Zadok***, avizadok@caltech.edu

Tuesday, May 5th

4:00pm-5:00pm.

Watson 104

Refreshments will be available in the Watson Lobby at 3:45pm